Electronic Acknowledgement Receipt

EFS ID:	2989013
Application Number:	10659974
International Application Number:	
Confirmation Number:	5045
Title of Invention:	CHANNEL BONDING OF A PLURALITY OF MULTI-GIGABIT TRANSCEIVERS
First Named Inventor/Applicant Name:	Joseph Neil Kryzak
Customer Number:	24309
Filer:	Justin Liu/Katherine Stofer
Filer Authorized By:	Justin Liu
Attorney Docket Number:	X-1367 US
Receipt Date:	12-MAR-2008
Filing Date:	11-SEP-2003
Time Stamp:	20:14:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810
RAM confirmation Number	4119
Deposit Account	240040
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

| 1 | Foreign Reference | EP_0315275_A2.pdf | 818323 | no | 12 |
| | | | 73f317b0444bbc3e9fc21c1081b241b1a52553fd | | |

Warnings:

Information:

| 2 | Foreign Reference | WO_9325968A1.pdf | 1145636 | no | 30 |
| | | | 5c1d69c81f63483fbe4dd8ce14482e80b4ce60cb | | |

Warnings:

Information:

| 3 | Foreign Reference | EP_0905906A2.pdf | 502067 | no | 10 |
| | | | 657533de778bc6b4b24e273f3aa34bbe7c2defa8 | | |

Warnings:

Information:

| 4 | Foreign Reference | EP_1235351A1.pdf | 505729 | no | 11 |
| | | | 04b5251e02b6872f6c304897a4addf27081508b4 | | |

Warnings:

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| 5 | NPL Documents | Albaharna_Area_and_Time_NPL.pdf | 501011 | no | 6 |
| | | | 9f15f918bd2cefdab1fe4a114c891b061fcf05a4 | | |

Warnings:

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| 6 | NPL Documents | Andrew_A_Field_Prog_NPL.pdf | 386491 | no | 5 |
| | | | 6398605495071dcfeb5e68c7140c8812f8da557e | | |

Warnings:

Information:

| 7 | NPL Documents | Carter_The_Future_of_Programmable_NPL.pdf | 586523 | no | 8 |
| | | | 210d3c698cec849d81abb395ffb8d79b76dbd35d | | |

Warnings:

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| 8 | NPL Documents | Davidson_FPGA_Implementation_NPL.pdf | 232306 | no | 4 |
| | | | 524ab3cf0f7e6fb9a92de39a854108065 72bec79 | | |

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| 9 | NPL Documents | DeHon_DPGA_Coupled_NPL.pdf | 798451 | no | 10 |
| | | | 8968c93265e94b334e824e21b8ccd2743218e374 | | |

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| 10 | NPL Documents | French_A_Self_reconfiguring_NPL.pdf | 813885 | no | 11 |
| | | | b9ce5be4dc79ed9424d5120cb0a4ebfad7b2f225 | | |

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| 11 | NPL Documents | IBM_32Bit_NPL.pdf | 6761375 | no | 140 |
| | | | 793b29adcaddb45f6a98e46eb1d0bdc5e59bbb9c | | |

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| 12 | NPL Documents | IBM_Powerpc_405_NPL.pdf | 18215204 | no | 550 |
| | | | ed60956e989f9ccf305fc5ef27eb91b9912c02a1 | | |

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| 13 | NPL Documents | Iseli_A_C_Plus_Plus_Compiler_NPL.pdf | 446551 | no | 8 |
| | | | 9fa4c11313f0224b55e1a6b75b52b3dc71a64792 | | |

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| 14 | NPL Documents | Iseli_Beyond_Superscaler_NPL.pdf | 255066 | no | 5 |
| | | | d238f4c62b2c2f762345270e1b3b3a6488265ed5 | | |

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| 15 | NPL Documents | Iseli_Spyder_A_Reconfigurable_NPL.pdf | 442425 | no | 8 |
| | | | 2994ae17276c44fe52b5aa9cabe792678fb1ee75 | | |

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| 16 | NPL Documents | Kiaei_VLSI_Design_of_Dynamically_NPL.pdf | 270396 | no | 5 |
| | | | ba6a993ec1586dcfb4e1e25f2f6afa59c83ce366 | | |

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| 17 | NPL Documents | Maki_A_Reconfigurable_Data_NPL.pdf | 256368 | no | 4 |
| | | | a8ae705c19884119a9eb3c1b5631bbab10d2ea48 | | |

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| 18 | NPL Documents | Snyder_Xilinxs_A_to_Z_NPL.pdf | 490110 | no | 5 |
| | | | 9301317c08b383e141187945eb0f7395587b9663 | | |

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19	NPL Documents	Srini_Field_Programmable_Gate_NPL.pdf	495908 8633b3fa7e243b32c998344abc18ff3f5 4e41b68	no	6

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20	NPL Documents	Wirthlin_The_Nano_Processor_NPL.pdf	711475 e070635b6cf8ef4a0a43626e2501bd36 cef563fb	no	10

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21	NPL Documents	Wittig_OneChip_an_FPGA_NPL.pdf	1023485 55e83f0f0cceeba4293cab4d520ba5afd 3c6069e	no	11

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22	NPL Documents	Xilinx_Programmable_LDB_1994_2_9_to_2_18_NPL.pdf	1066027 6417934074352e160802dbed12a9915 e9ed63452	no	13

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23	NPL Documents	Xilinx_Programmable_LDB_1994_2_107_to_2_108_NPL.pdf	331834 629220e381350b732457199ee5896aef 39f3f57c	no	5

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24	NPL Documents	Xilinx_Programmable_LDB_1994_2_109_to_2_117_NPL.pdf	773523 299459636bd2270814c3b678ebc1764 e5dd2d328	no	12

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25	NPL Documents	Xilinx_Programmable_LDB_1994_2_187_to_2_199_NPL.pdf	1156817 037a187122468d0c0cab8f2b5a5f7124 eff89f7f	no	16

Warnings:

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26	NPL Documents	Xilinx_Programmable_LDB_1999_3_1_to_3_50_NPL.pdf	3031136 f00143b2ff352e3d69a480d4689785bbe 3721421	no	54

Warnings:

Information:

27	NPL Documents	Xilinx_Programmable_LDB_2000_3_1_to_3_117_NPL.pdf	7056683 664bd6fb7e119b956ff0204ec75248ad5 a26471d	no	122

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28	NPL Documents	Xilinx_Programmable_LDB_2000_3_7_to_3_87_NPL.pdf	2219494 494786481dbd3ed351f72f9667b55021651ea933	no	27

Warnings:

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29	NPL Documents	Xilinx_Virtex_Two_PLatform_FPGA_Hndbk_NPL.pdf	3105531 246f66d95af30e27f3628189328bb1b85f5614ab	no	45

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Information:

30	NPL Documents	Yamin_Aizup_A_Pipelined_NPL.pdf	501670 026d38abdaa5f96aca1ee112a14ed3e58c972a1a	no	9

Warnings:

Information:

31	NPL Documents	Xilinx_Programmable_LDB_1994_rv_1995_Part1_pgs_1_to_345_NPL.pdf	21297550 6d73fe5733521ccc6986c2f3f53803bfce43c3ca	no	345

Warnings:

Information:

32	NPL Documents	Xilinx_Programmable_LDB_1994_rv_1995_Part2_pgs_346_to_689_NPL.pdf	20651519 c60d88b085770d8ae93953546d234b9bf2eb64c7	no	344

Warnings:

Information:

33	Request for Continued Examination (RCE)	X1367_US_RCE_wIDS_efiled.pdf	627252 2251cef587c82d610ec2c2bff59bfd4641ecfe91	no	3

Warnings:

Information:

34	Information Disclosure Statement (IDS) Filed	X1367_US_SB08A_efiled.pdf	130890 5a374aac92d90d529c1466f84e498240dd33bdd2	no	7

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Information:

This is not an USPTO supplied IDS fillable form

35	Fee Worksheet (PTO-06)	fee-info.pdf	8205 ec0f47b3633bf36e588d955414a32806dd12934c	no	2

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		Total Files Size (in bytes):	97616916

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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